PATENT COOPERATION TREATY

PCT/JP2003/015838

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference					
P0656PC	FOR FURTHER A	CTION	See Form PCT/IPEA/416		
International application No. PCT/JP2003/015838	International filing da 11 December 20	03 (11 12 2002)	Priority date (day/month/year)		
International Patent Classification (IPC) or na G06F 9/46	tional classification an	d IPC	09 January 2003 (09.01.2003)		
Applicant JAPAN	SCIENCE AND TI	ECHNOLOGY AG	GENCY		
 This report is the international prelim Authority under Article 35 and transn 	nary examination repo itted to the applicant a	rt, established by this ccording to Article 36	International Preliminary Examining		
 This REPORT consists of a total of _ This report is also accompanied by AN 	4 sheets,	ncluding this cover sh	neet.		
a. (sent to the applicant and to	the International Bure	cau) a total of 13	sheets as follows:		
sheets of the descrip and/or sheets contain Administrative Instruction Sheets which supersonable beyond the disclosure Supplemental Box.	tion, claims and/or dra ning rectifications auth actions). ade earlier sheets, but e in the international a	wings which have bee orized by this Author which this Authority of application as filed, as	en amended and are the basis of this report ity (see Rule 70.16 and Section 607 of the considers contain an amendment that goes indicated in item 4 of Box No. I and the		
Administrative Instructions).	ated in the Supplemer	ital Box Relating to S	and number of electronic carrier(s)) and/or tables related thereto, in computer Sequence Listing (see Section 802 of the		
4. This report contains indications relating Box No. I Basis of the report		:			
Box No. I Basis of the repor					
	of opinion with recar	d to novelby impact			
Box No. IV Lack of unity of in	Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability Lack of unity of invention				
		vith regard to novelty, h statement	inventive step or industrial applicability;		
Box 140. VI Certain documents	cited				
	Certain defects in the international application				
	s on the international a	application			
ate of submission of the demand		te of completion of th	is report		
07 April 2004 (07.04.2004			ust 2004 (23.08.2004)		
me and mailing address of the IPEA/JP	Au	horized officer	(-2.00.2004)		
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Translation

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.

Box No. I Basis of the report	TOTAL ON PATENTABILITY	PCT/JP2003/015838
	nort is based on the t	
otherwise indicated under this item.	port is based on the international application in the la	anguage in which it was filed, unless
This report is based on trans	lations from the original language into the followi tion furnished for the purpose of:	ing language
international search (und	ler Rules 12.3 and 23.1(b))	
publication of the interna	ational application (under Rule 12.4)	
international preliminary	examination (under Rules 55.2 and/or 55.3)	
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2. With regard to the elements of the	international application, this report is based on asponse to an invitation under Article 14 are referen	
and are not annexed to this report):	international application, this report is based on isponse to an invitation under Article 14 are refern	replacement sheets which have beer ed to in this report as "originally flation."
The international application as	Originally filed/5	originally filed
the description:	ong many mea/turnished	
pages	1-13	
pages*	received by this Authority on	, as originally filed/furnish
pages*	received by this Authority on	
the claims:	and by this Authority on	
pages	50.11.12	
pages*	5-9, 11-13	, as originally filed/furnishe
pages* 1-3, 10, 14	, as amended (toge	ether with any statement) under Article
pages*	received by this Authority on received by this Authority on	23 July 2004 (23.07.2004)
the drawings:	on	
pages	1.0	
pages*	1-8	, as originally filed/furnished
pages*	received by this Authority on received by this Authority on	
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mwo moung mwo any relati	ed table(s) - see Supplemental Box Relating to Sequ	uence Listing.
The amendments have required in		
The state of the s	the cancellation of:	
the description, pages		
the claims, Nos.	. 4	
the drawings, sheets/figs		
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any table(s) related to sequen	ce listing (specify):	
	we to pecify.	
This report has been		
made, since they have been considered	if (some of) the amendments annexed to this repo dered to go beyond the disclosure as filed as inc	ort and listed below had not have
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the description, pages		
the drawings, sheets/figs		
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tem 4 applies, some or all of those sheets		j.
PCT/IPEA/409 (Box No. I) (January 200	04)	
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Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

tatement			
Novelty (N)	Claims	1-3, 5-15	YES
	Claims		МО
Inventive step (IS)	Claims		YES
	Claims	1-3, 5-15	NO
Industrial applicability (IA)	Claims	1-3, 5-15	YES
	Claims		NO

2. Citations and explanations (Rule 70.7)

Document 1: "Parallel Replacement Mechanism for MultiThread, Advances in Parallel and Distributed Computing," (C. Guangzuo, et al.), 1997 Proceedings, 1997, pages 338-343; especially see page 340 and Figure 31

Document 2: "Pica: An Ultra-Light Processor for High-Throughput Application, Computer Design: VLSI in Computers and Processors," (D. S. Wills, et al.), 1993 ICCD '93 Proceedings, 1993, pages 410-414; especially see pages 411-412

Document 3: JP, 2002-533807, A (Koninklijke Philips Electronics N.V.), 8 October, 2002, (08.10.02), paragraphs [0010]-[0016]

Document 4: JP, 2002-513182, A (Infineon Technologies North America Corp.), 8 May, 2002 (08.05.02), page 12, line 14 to page 17, line 9

Document 5: JP, 3-9431, A (NEC Corp.), 17 January, 1991 (17.01.91), full text

Claims 1-3, 5, 10, 11, 14 and 15

Document 1 discloses a context changeover apparatus connected to a register (register file) and comprising (1) a restore bus and a save bus, (2) two temporary register sets (temporary register sets) for temporarily buffering contexts and (3) a control unit (thread control unit), for concurrently executing the saving and restoring of contexts through the restore bus and the save bus.

Document 2 discloses a technique in which (1) a context is searched based on a context ID (thread identifier), for specifying the context to be replaced, and (2) a context cache is accessed. Furthermore, being single cycle task swaps is described.

Document 3 also discloses a technique for managing a context for each thread as in document 2, and it is considered to be obvious for a person skilled in the art to manage contexts based on thread identifiers, based on this description. Furthermore, the document describes that it is suitable that a processor, a memory and buses are formed on a common silicon board. (Document 3 also discloses the relation between threads and the addresses in a cache, though this is not clear in the claims of the present application.)

The temporary register sets and the main memory where contexts are finally stored, disclosed in document 1, are considered as kinds of context caches. In this case, the constitution, in which a read port and a write port are established in correspondence to a restore bus and a save bus, is considered to be obvious for a person skilled in the art.

Furthermore, the constitution, in which threads and contexts are related to each other using thread identifiers for management, is described in documents 2 and 3. Moreover, a person skilled in the art could have easily mounted a context cache as a chip in a central processing unit, from the description of document 3.

Therefore, a person skilled in the art could have easily arrived at the subject matters of claims 1-3, 5, 10, 11, 14 and 15 based on the descriptions of documents 1-3.

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient. Continuation of: V

Claims 8 and 9

Document 4 discloses a microprocessor comprising an instruction control unit 101, an integer execution unit 102, a load/store unit 103, an instruction memory 300, a data memory 200, and a peripheral unit 400. A person skilled in the art could have easily installed an instruction cache, data cache, instruction fetch unit, arithmetic and logic unit, memory access unit, and arithmetic bus based on the description of document 4, in the context changeover apparatus that a person skilled in the art could have easily conceived of from the already discussed documents 1-3.

Claims 6, 7, 12 and 13

Document 5 discloses a technique for issuing a save instruction (backup instruction) and a restore instruction (restore instruction) for switching contexts. A person skilled in the art could have easily installed the above instructions described in document 5 in the context changeover apparatus that a person skilled in the art could have easily conceived of from the already discussed documents 1-4.